REMARKS

The Examiner rejected claims 1-35 under 35 U.S.C. 112 as containing insufficient antecedent basis. Claims 1, 2, 9, 17, 35, and 36 have been amended to clarify claim language and address this concern. No new matter has been added. These amendments should render moot the Examiner's further rejection of claims 2-8, 10-16, and 18-34 for incorporating the previous alleged deficiency of the parent claims. These amendments were not made for any prior art reasons and the full range of equivalents, for all claims, should remain intact.

The Examiner rejected claims 1, 3, 4, 9, 11, 12, 17-19, 21-24, and 29-36 under 35 U.S.C. 102(b) as being anticipated by Cohn et al. (U.S. Patent No. 5,734,861). These rejections are respectfully disagreed with, and are traversed below. The independent claims at issue are claims 1, 9, 17, 35, and 36, to which the remarks below are primarily directed.

Although Cohn et al. disclose the use of two least recently used (LRU) lists to reference dirty data and clean data in the data cache, the conditions for destaging dirty data and purging clean data are clearly different and unique between Cohn et al. and the subject application.

Cohn et al. disclose the use of two LRU lists to reference data in the log-structured array (LSA) cache memory, as evident in Fig. 4, col. 6, lines 53-56, and col. 9, lines 39-46. At col. 6, lines 56-62, Cohn et al. state:

> The LSA cache memory is maintained by the LSA controller so the controller knows the fraction of cache memory occupied by dirty tracks. **When this fraction exceeds a predetermined dirty track threshold, a dirty track is moved from the LSA cache memory to the memory segment**, where they get written to disk. This operation is referred to as destaging the LSA cache. (emphasis added)

The method employed by Cohn et al. destages the LSA cache when the fraction of cache memory occupied by dirty tracks exceeds a predetermined threshold.

In comparison, currently amended claim 1 of the subject application states:

> ...wherein **the dirty data is destaged from the data cache when the dirty data reaches the tail of the first least recently used list** and the clean data is purged from the data cache when the clean data reaches the tail of the second least recently used list. (emphasis added)

The program, system, and method taught by the subject application destage the data cache when the dirty data reaches the tail of the first LRU list.

The Examiner cites Cohn et al. at col. 7, lines 10-15 and col. 12, lines 60-65 as disclosing that dirty data is destaged from the data cache when the dirty data reaches the tail of the first recently used list and the clean data is purged from the data cache when the clean data reaches the tail of the second least recently used list. The Applicants respectfully disagree with the Examiner's interpretation of the teachings of Cohn et al.

At col. 7, lines 9-12, Cohn et al. state:

> ...shortly before the space containing an LRU clean track is to be written back and reused, meaning that the logical track is at the bottom of the clean track LRU list...

Here, Cohn et al. are not specifying *when* a clean track is purged from the clean track LRU list but rather *where* the track-to-be-purged is located on the clean track LRU list.

At col. 12, lines 57-63, Cohn et al. state:

> As noted above, destaging is begun if the percentage of dirty tracks exceeds a start threshold value. The first step of the destaging operation, indicated by the FIG. 7 flow diagram box numbered 140, is to identify an updated track to be moved from the LSA cache memory to the memory segment. Typically, the updated track to be moved is the bottom track entry in the dirty track LRU list.

Again, when referring to the bottom track entry of the dirty track LRU list, Cohn et al. are not disclosing what condition must be met for the dirty track to be destaged but rather where the to-be-destaged dirty track "typically" is located.

Additional references to the destaging condition required by Cohn et al. may be found in the figures of the patent. In Fig. 6, decision box 128 asks:

> Does percentage of cache that is dirty exceed the dirty cache destaging start threshold?

Whereupon the answer is "yes," the flow diagram proceeds to box 130 in which the LSA controller begins the destaging process. (See col. 12, lines 12-20 of Cohn et al.)

Similarly, decision box 149 in Fig. 7 of Cohn et al. inquires:

> Destaging stop threshold value met?

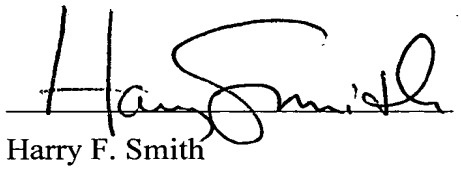
Should the answer be in the affirmative, the LSA controller ceases the destaging process. (See col. 13, lines 8-17 of Cohn et al.)

Clearly, Cohn et al. teach that dirty data be destaged when the fraction of cache memory occupied by dirty tracks exceeds a predetermined threshold and *not* that "the dirty data is destaged from the data cache when the dirty data reaches the tail of the first least recently used list," as is recited in, for example, claims 1, 9, 17, 35, and 36 of the subject application.

Based upon the foregoing, the disclosure in Cohn et al. cited by the Examiner cannot be seen to anticipate, and thus render unpatentable, claims 1, 9, 17, 35, and 36 of the subject application. In that claims 1, 9, 17, 35, and 36 are patentable over Cohn et al., then at least for this reason claims 3, 4, 11, 12, 18, 19, 21-24, and 29-34 are also patentable. Similarly, the Examiner's objections to claims 2, 5-8, 10, 13-16, 20, and 25-28 as being dependent upon rejected base claims are also addressed.

The Examiner is respectfully requested to reconsider and remove the rejection of claims 1-35 under 35 U.S.C. 112, the rejection of claims 1, 3, 4, 5, 11, 12, 17-19, 21-24, 29-36 under 35 U.S.C. 102(b), and the objection to claims 2, 5-8, 10, 13-16, 20, and 25-28 for dependency upon a rejected base claim, and to allow all of the pending claims 1-36 as now presented for examination. An early notification of the allowability of claims 1-36 is earnestly solicited.

Respectfully submitted:



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Harry F. Smith Date

Reg. No.: 32,493

Customer No.: 29683

HARRINGTON & SMITH, LLP
4 Research Drive
Shelton, CT 06484-6212

Telephone: (203)925-9400
Facsimile: (203)944-0245
email: hsmith@hspatent.com

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